IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Dennis M. O'Connor	Atty. Docket No: 42P15392
Application No.: 10/773,847	Art Unit: 2186
Filed: February 5, 2004	Confirmation No.: 7172
Title: ADDRESS CONVERSION TECHNIQUE IN A CONTEXT SWITCHING ENVIRONMENT	Examiner: Pierre Miche Bataille

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Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

IN SUPPORT OF APPELLANT'S APPEAL

TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

In response to the Final Office Action dated February 26, 2007 and pursuant to Appellant's Notice of Appeal filed on May 25, 2007, Appellant presents this Brief and fee under 37 C.F.R. § 1.17(c) in appeal of the Final Rejection dated February 26, 2007.

I. REAL PARTY IN INTEREST.

Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES.

There are no related appeals or interferences before the Board of Patent Appeals and Interferences known to Appellant, the Appellant's legal representatives, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS.

A total of claims 1-24 have been pending in the application and their status is as follows:

Claims 1-24 stand finally rejected and are the claims subject to this appeal. The claims appendix includes a copy of the claims subject to this appeal.

The rejections of independent claim 1 and its dependent claims, independent claim 11 and its dependent claims, and independent claim 17 and its dependent claims are appealed.

IV. STATUS OF AMENDMENTS.

All amendments filed to date have been entered into the record. No amendment after final was made.

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Embodiments of the present invention relate to a memory management unit (Fig. 2). The memory management unit stores generated virtual address-to-physical address translations. If a virtual address-to-physical address translation is available for a particular virtual address, the memory management unit retrieves the corresponding physical address. If a translation is not available, the memory management unit generates the corresponding physical address from the virtual address. The memory management unit converts the virtual address to a modified virtual address using a process identifier and then performs a page table walk using the modified virtual address, generating the physical address. Paragraph [1009]

Referring to Appellant's independent claim 1, by way of example, a memory management unit is claimed. (Fig. 2; paragraph [1018]) The memory management unit is configured to receive a virtual address and provide a corresponding physical address. (Fig. 2; paragraph [1018]) The memory management unit includes a storage containing one or more virtual address-to-physical address translations. (Fig. 2, 202; paragraph [1018]) The memory management unit also includes conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage. (Fig. 2, 206; paragraph [1018]) The memory management unit also includes a page table walk unit configured to convert the modified virtual address into the corresponding physical address. (Fig. 2, 208; paragraph [1020])

Referring to independent claim 12, by way of example, a system is claimed. (Fig. 1; paragraph [1015]) The system includes an antenna, (Fig. 1, 108; paragraph [1017]), a memory (Fig. 1, 106; paragraph [1016]), and a processor coupled to the antenna and memory (Fig. 1, 100; paragraph [1016]). The processor includes an address generation unit (Fig. 1, 102; paragraph [1015]) and a memory management unit (Fig. 1, 104; paragraph [1015]). The memory management unit is configured to receive a virtual address from the address generation unit and provide a corresponding physical address (Fig. 2; paragraph [1018]). The memory management unit includes a storage containing one or more virtual address-to-physical address translations (Fig. 2, 202; paragraph [1018]); conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage (Fig. 2, 206; paragraph [1018]); and a page table walk unit configured to convert the modified virtual address into the corresponding physical address (Fig. 2, 208; paragraph [1020]).

Referring to independent claim 17, by way of example, a method is claimed. The method includes receiving a virtual address at a memory management unit (Fig. 2; paragraph [1018]); determining if the virtual address has a translation to a physical address in a storage (Fig. 2, 202; paragraph [1018]); if not, generating a modified virtual address from the virtual address (Fig. 2, 206; paragraph [1018]); and translating the modified virtual address into a physical address (Fig. 2, 208; paragraph [1020]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.

The issues for consideration on this appeal are:

A. Whether the Examiner erred in rejecting independent claims 1, 11, and 17, and their respective dependent claims 2-10, 12-16, and 18-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,754,784 to North et al. (hereinafter "North") in view of Day et al., U.S. Patent Publication No. 2004/0117592 (hereinafter "Day").

VII. ARGUMENT.

A. Claims 1-24 are patentable under 35 U.S.C. §103(a) over North in view of Day.

Claims 1 - 24 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over North in view of Day. Appellant respectfully requests that these rejections be overturned for the following reasons.

It is well established that a *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. MPEP 2142.

The Final Office Action dated 2/26/07 has failed to present a *prima facie* case of obviousness for claims 1-24.

1. Neither North nor Day, or North and Day combined, teach or suggest all claim limitations.

Claim 1 recites: "conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage." Independent claims 11 and 17 recite limitations that are similar to the limitations of claim 1, although some differences may exist among the limitations.

The Final Office Action states that the "access control logic for the translation of virtual addresses into modified virtual addresses" disclosed by North at Col. 3, lines 48-66, is equivalent to the "conversion logic to generate a modified virtual address from the virtual address" as claimed in claim 1. Final Office Action, page 3, lines 14-16. However the "access control logic" disclosed by North does not generate a modified virtual address from a virtual address as claimed in claims 1, 11, and 17.

North teaches a memory management unit (MMU) 104 which includes a translation look aside buffer (TLB), access control logic, and translation table walking logic. Fig. 2; Col. 3, lines 48-50. The primary functions of the MMU 104 are: 1) the translation of virtual addresses into physical addresses; and 2) the control of accesses to memory. Col. 3, lines 50-52. The translation look aside buffer (TLB) encaches translated entries and provides the translation to the associated access control logic. Col. 3, lines 53-55. If a virtual address causes a hit to a

translated physical address entry in the TLB, the access control logic determines whether the access to the physical address is permitted. Col. 3, lines 55-57. Thus, the access control logic of North does not generate a modified virtual address. The access control logic of North only determines whether access to a physical address is permitted after the virtual address has been translated to a physical address by the TLB. North's TLB provides virtual-to-physical address translation. The access control logic determines whether access to the physical address is permitted. The access control logic does not generate any type of address. Moreover, North does not teach or suggest a modified virtual address. North discloses only translation of virtual addresses into physical addresses. Thus, North does not teach or suggest "conversion logic to generate a modified virtual address from the virtual address," as claimed in claim 1.

Day also does not teach or suggest "conversion logic to generate a modified virtual address from the virtual address," as claimed in claim 1." Day discloses a page replacement algorithm (PRA) to assist a TLB when there is a TLB miss. Paragraph [0017]. Day's computer system has a first memory to store address translation information between virtual addresses and real addresses. The second memory caches at least part of the address translation information for faster access from the processing logic. Paragraph [0009]. Day does not teach or suggest a modified virtual address, nor does Day teach or suggest "conversion logic to generate a modified virtual address from the virtual address."

Thus, neither North nor Day teach or suggest at least "conversion logic to generate a modified virtual address from the virtual address." Because taken alone or in combination the

cited references fail to teach or suggest each and every claim limitation of independent claims 1, 11, and 17, and their respective dependent claims 2-10, 12-16, and 18-24, Appellant respectfully submits that a *prima facie* case of obviousness under 35 U.S.C. §103(a) has not been established. Accordingly, reconsideration and withdrawal of these rejections are respectfully requested.

For at least the foregoing reasons, the 35 U.S.C. §103(a) rejection of independent claims 1, 11, and 17 should be withdrawn and these claims should be allowed to issue. In addition, claims 2-10, 12-16, and 18-24, which depend from claims 1, 11, and 17, respectively, should also be allowed for at least the foregoing reasons.

Conclusion

Appellant respectfully submits that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 50-0221.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. (Previously presented) A memory management unit configured to receive a virtual address and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

2. (Original) The memory management unit as recited in Claim 1, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits comprises a predetermined value.

3. (Original) The memory management unit as recited in Claim 2, wherein the predetermined value is zero.

4. (Original) The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an arithmetic logic unit.

5. (Original) The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an incrementor.

6. (Original) The memory management unit as recited in Claim 1, wherein the virtual address comprises a data address.

7. (Original) The memory management unit as recited in Claim 1, wherein the virtual address comprises an instruction address.

8. (Original) The memory management unit as recited in Claim 1, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

9. (Original) The memory management unit as recited in Claim 1, wherein only virtual address-to-physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

10. (Original) The memory management unit as recited in Claim 1, wherein the storage is configured to store one or more most recently generated virtual address-to-physical address translations.

11. (Previously presented) A system comprising:

an antenna;

a memory; and

a processor coupled to the antenna and memory, the processor comprising:

an address generation unit; and

a memory management unit configured to receive a virtual address from the address generation unit and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

12. (Original) The system as recited in Claim 11, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

13. (Original) The system as recited in Claim 11, wherein the address generation unit comprises an arithmetic logic unit.

14. (Original) The system as recited in Claim 11, wherein the address generation unit comprises an incrementor.

15. (Original) The system as recited in Claim 11, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

16. (Original) The system as recited in Claim 11, wherein only virtual address-to-physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

17. (Previously presented) A method comprising:

receiving a virtual address at a memory management unit;

determining if the virtual address has a translation to a physical address in a storage;

if not, generating a modified virtual address from the virtual address; and

translating the modified virtual address into a physical address.

18. (Original) The method as recited in Claim 17, wherein generating the modified virtual address comprises replacing one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

19. (Original) The method as recited in Claim 17, wherein translating the modified virtual address comprises performing a page table walk.

20. (Original) The method as recited in Claim 17, further comprising invalidating all translations in the storage if a process identifier changes.

21. (Original) The method as recited in Claim 17, further comprising invalidating only translations in the storage having a virtual address portion that has one or more bits equal to a predetermined value.

22. (Original) The method as recited in Claim 17, further comprising placing any generated translations into the storage.

23. (Original) The method as recited in Claim 17, wherein the virtual address is a data address.

24. (Original) The method as recited in Claim 17, wherein the virtual address is an instruction address.

IX. EVIDENCE APPENDIX

Not Applicable

X. RELATED PROCEEDINGS APPENDIX

Not Applicable